EJ

Notice of Allowability	Application No.	Applicant(s)	
	10/659,337	HAEMATSU, HITOSHI	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the filing of the RCE on 3 January 2006*.

2. ☒ The allowed claim(s) is/are *1-4*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Michael Trinh
Primary Examiner

DETAILED ACTION

This office action is in response to the filing of the RCE on 3 January 2006.

Claims 1-4 are pending.

Allowable Subject Matter

Claims 1-4 are allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: prior art does not anticipate, teach, or suggest a manufacturing method of a semiconductor device where a plurality of electrodes are formed on a front face of a semiconductor chip; covering the front face of the semiconductor chip with a resin insulating film; covering all of an upper surface and side surfaces of the resin insulating film with a metal protective film so that the metal protective film contacts the resin insulating film and extends to a surface of the semiconductor chip; and providing an electrical connecting portion at a reverse face of the semiconductor chip, wherein the electrical connecting portion is connected to at least any of the plurality of electrodes on the front face of the semiconductor chip.

For example, Harumi (JP 61019154) discloses a manufacturing method of a semiconductor device where an electrode is formed on a front face of a semiconductor chip; covering the front face the semiconductor chip with a resin insulating film; and

covering all of an upper surface and side surfaces the resin insulating film with a metal protective film.

However, Harumi does not disclose, anticipate, teach, or suggest covering all of an upper surface and side surfaces of the resin insulating film with a metal protective film so that the metal protective film contacts the resin insulating film and extends to a surface of the semiconductor chip; and providing an electrical connecting portion of at least any of the plurality of electrodes at a reverse face of the semiconductor chip.

Hajime (JP 08107120) discloses a manufacturing method of a semiconductor device where a plurality of electrodes are formed on front face of a semiconductor chip; covering the front face of the semiconductor chip with a metal protective film, wherein a space is left between the front face of the semiconductor chip and the metal protective film; and providing an electrical connecting portion of at least any of the plurality of electrodes at a reverse face of the semiconductor chip.

However, Hajime does not disclose, anticipate, teach or suggest covering the front face of the semiconductor chip with a resin insulating film; and covering all of an upper surface and side surfaces of the resin insulating film with a metal protective film so that the metal protective film contacts the resin insulating film and extends to a surface of the semiconductor chip.

The prior art made of record in this action does not anticipate, teach, or suggest a manufacturing method of a semiconductor device where a plurality of electrodes are formed on a front face of a semiconductor chip; covering the front face of the semiconductor chip with a resin insulating film; covering all of an upper surface and side

surfaces of the resin insulating film with a metal protective film so that the metal protective film contacts the resin insulating film and extends to a surface of the semiconductor chip; and providing an electrical connecting portion at a reverse face of the semiconductor chip, wherein the electrical connecting portion is connected to at least any of the plurality of electrodes on the front face of the semiconductor chip.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

Michael Trinh
Primary Examiner